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Karen Cinq-Mars  
Karen Cinq-Mars  
(Signature)

7/18/03

(Date)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of : July 18, 2003  
Chen et al. :  
Serial No. : Examiner:  
Filed: Herewith : IBM Corporation  
Title: IMPROVED VERTICAL MOSFET  
WITH DUAL WORK FUNCTION  
MATERIALS : Dept. 18G/Bldg. 300-482  
2070 Route 52  
Hopewell Junction,  
New York 12533-6531

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

Sir:

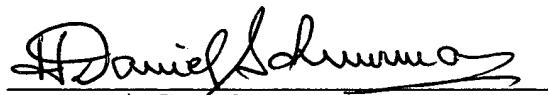
In compliance with the duty of disclosure under  
37 C.F.R. § 1.56 and in accordance with the practice under  
37 C.F.R. §§ 1.97 and 1.98, the Examiner's attention is directed to  
the documents listed on the enclosed Form PTO-1449. Copies of the  
listed documents are also enclosed.

It is respectfully requested that the above information be  
considered by the Examiner and that a copy of the enclosed Form  
PTO-1449 be returned indicating that such information has been  
considered.

Applicants' undersigned attorney may be reached by telephone

at (845) 894-2481. All correspondence should continue to be directed to the below listed address.

Respectfully submitted,

  
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Patent Agent  
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FIS920030102US1

<b>INFORMATION DISCLOSURE CITATION</b> <i>(Use several sheets if necessary)</i>				Docket Number (Optional) <b>FIS920030102US1</b>		Application Number	
				Applicant(s) <b>Chen et al.</b>			
				Filing Date		Group Art Unit	
<b>U.S. PATENT DOCUMENTS</b>							
*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
<b>FOREIGN PATENT DOCUMENTS</b>							
REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation	
						YES	NO
<b>OTHER DOCUMENTS</b> <i>(Including Author, Title, Date, Pertinent Pages, Etc.)</i>							
		H. Akatsu et al., "A highly manufacturable 110nm DRAM technology with 8F2 vertical transistor cell for 1Gb and beyond", IEEE 2002 Symposium on VLSI Technology Digest of Technical Papers					
		K. McStay et al., "Vertical pass transistor design for sub-100nm DRAM technologies", IEEE 2002 Symposium on VLSI Technology Digest of Technical Papers					
		J. A. Mandelman et al., "Challenges and future directions for the scaling of dynamic random-access memory (DRAM)", IBM Journal of Research and Development, Vol. 46, No. 2/3, March/May 2002, pp. 187 - 208					
EXAMINER				DATE CONSIDERED			
<b>EXAMINER:</b> Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							